Digital System Design

Lecture 12

Combinational Logic Design

Binary Adder-Subtractor

Objectives:

1. **Half Adder.**
2. **Full Adder.**
3. **Binary Adder.**
4. **Binary Subtractor.**
5. **Binary Adder-Subtractor.**

1. Half Adder

Half Adder: is a combinational circuit that performs the addition of two bits, this circuit needs two binary inputs and two binary outputs.

Inputs		*Outputs*	
X	*Y*	*C*	*S*
0	*0*	*0*	*0*
0	*1*	*0*	*1*
1	*0*	*0*	*1*
1	*1*	*1*	*0*

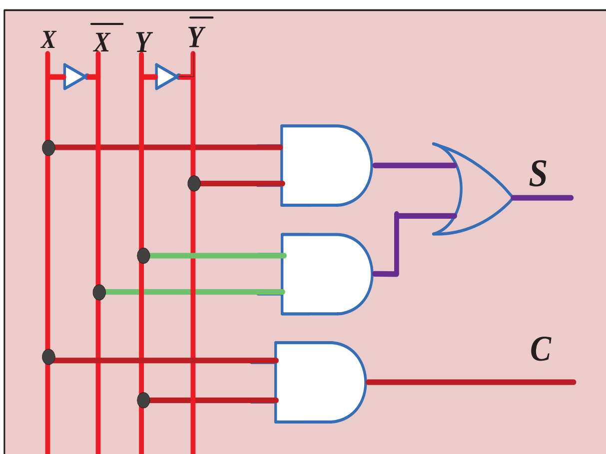
Truth table

The simplified Boolean function from the truth table:

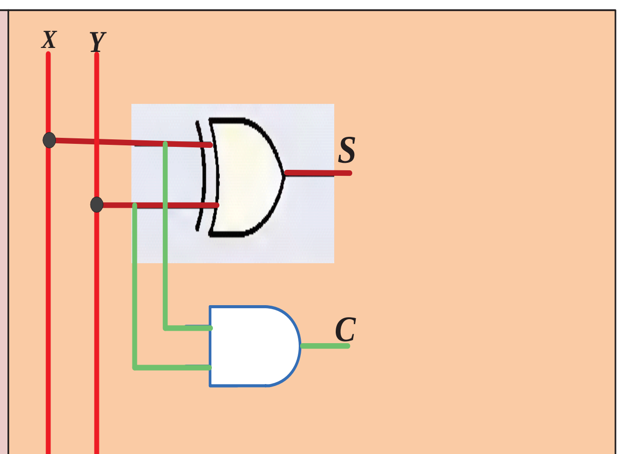
$$\left\{\begin{array}{l} S = \overline{X}Y + X\overline{Y} \\ C = XY \end{array}\right. \qquad 1\Big\} \text{ (Using sum of product form)}$$

Where S is the sum and C is the carry.

$$\left\{\begin{array}{l} S = X \oplus Y \\ C = XY \end{array}\right. \qquad 2\Big\} \text{ (Using XOR and AND Gates)}$$



Implementation of Half Adder using equation (1)



Implementation of Half Adder using equation (2)

- The implementation of half adder using ***exclusive–OR*** and an ***AND*** gates is used to show that two half adders can be used to construct a full adder.
- The inputs to the ***XOR*** gate are also the inputs to the ***AND*** gate.

2. Full Adder

Full Adder is a combinational circuit that performs the addition of three bits (two significant bits and previous carry).

- It consists of ***three inputs and two outputs***, two inputs are the bits to be added, the third input represents the carry form the previous position.
- The full adder is usually a component in a cascade of adders, which add 8, 16, etc, binary numbers.

Inputs			Outputs	
X	Y	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Truth table for the full adder

- The S output is equal to *1* when only one input is equal to *1* or when all three inputs are equal to *1*.
- The C_{out} output has a carry *1* if two or three inputs are equal to *1*.
- The Karnaugh maps and the simplified expression are shown in the following figures:

$X \backslash YC_{in}$	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$$S = \overline{X}\,\overline{Y}C_{in} + \overline{X}Y\overline{C_{in}} + X\overline{Y}\,\overline{C_{in}} + XYC_{in}$$

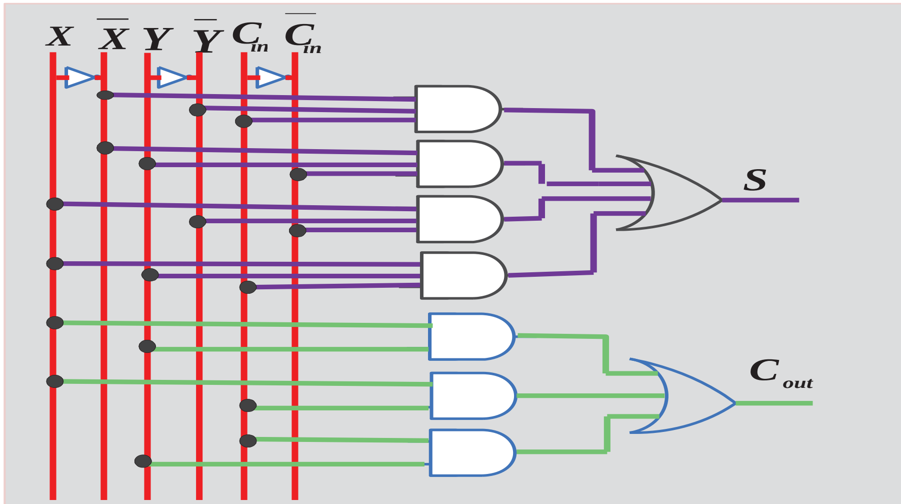
$X \backslash YC_{in}$	00	01	11	10
0	0	0	1	0
1	0	1	1	1

$$C_{out} = XY + XC_{in} + YC_{in}$$

$$\left.\begin{cases} S = \overline{X}\,\overline{Y}C_{in} + \overline{X}Y\overline{C_{in}} + X\overline{Y}\,\overline{C_{in}} + XYC_{in} \\ C_{out} = XY + XC_{in} + YC_{in} \end{cases}\right\} \quad 1$$

(Sum of products)

- The ***logic diagrams*** for the full adder implemented in ***sum-of-products*** form are the following:



logic diagram for the full adder

- It can also be implemented using ***two half adders*** and ***one OR gate*** (using ***XOR*** gates).

$$\begin{Bmatrix} S = C_{in} \oplus (X \oplus Y) \\ C_{out} = C_{in} \cdot (X \oplus Y) + XY \end{Bmatrix}$$

Proof:

The sum:

$$\mathbf{S} = \bar{X}\,\bar{Y}C_{in} + \bar{X}Y\overline{C_{in}} + X\bar{Y}\,\overline{C_{in}} + XYC_{in}$$

$$= \overline{C_{in}}(\bar{X}Y + X\bar{Y}) + C_{in}(\bar{X}\,\bar{Y} + XY)$$

$$= \overline{C_{in}}(\bar{X}Y + X\bar{Y}) + C_{in}\overline{(\bar{X}Y + X\bar{Y})}$$

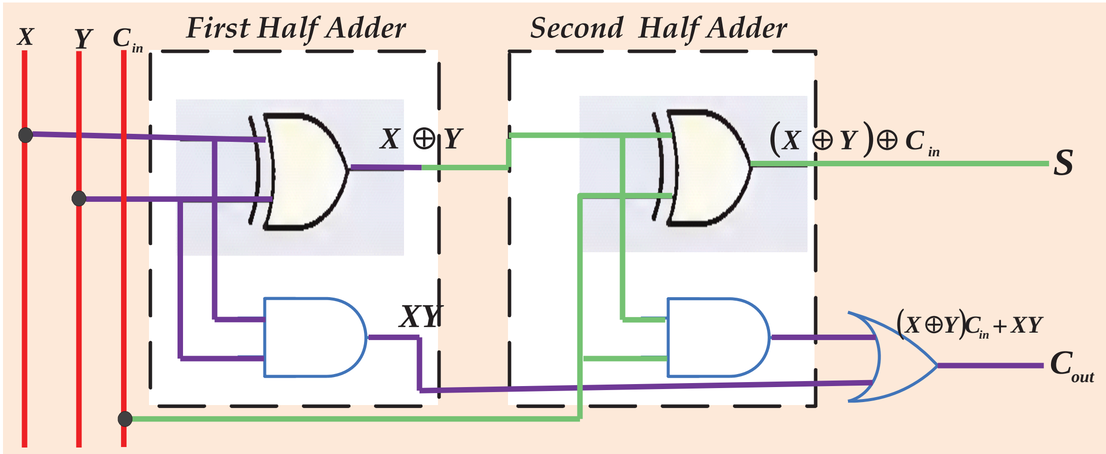
$$S = C_{in} \oplus (X \oplus Y)$$

The carry output:

$$C_{out} = \bar{X}YC_{in} + X\bar{Y}C_{in} + XYC_{in} + XY\,\overline{C_{in}}$$

$$= C_{in}(\bar{X}Y + X\bar{Y}) + XY(C_{in} + \overline{C_{in}})$$

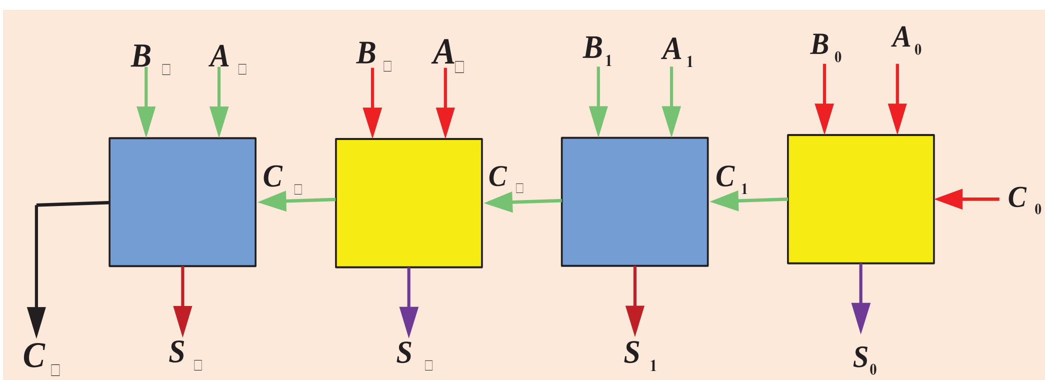
$$C_{out} = C_{in} \cdot (X \oplus Y) + XY$$



Implementation of Full Adder with two Half Adders and an OR gate

3. Binary Adder (Asynchronous Ripple-Carry Adder)

- A binary adder is a digital circuit that produces the ***arithmetic sum of two binary numbers***.
- A binary adder can be constructed with ***full adders connected in cascade*** with the output carry form each full adder connected to the input carry of the next full adder in the chain.
- The ***four-bit adder*** is a typical example of a ***standard component*** .It can be used in many application involving arithmetic operations.



Four-bit Adder (Ripple Carry Adder)

- The input carry to the adder is C_0 and it ripples through the full adders to the output carry C_4.
- n-bit binary adder requires n full adders.