7 Field Effect Transistor

7.1 INTRODUCTION

The FET is a device in which the flow of current through the conducting region is controlled by an electric field. Hence the name Field Effect Transistor (FET). As current conduction is only by majority carriers, FET is said to be a unipolar device.

Based on the construction, the FET can be classified into two types as *Junction FET (JFET)* and *Metal Oxide Semiconductor FET (MOSFET)* or *Insulated Gate FET (IGFET)* or *Metal Oxide Silicon Transistor (MOST)*.

Depending upon the majority carriers, JFET has been classified into two types, namely, (1) *N-channel JFET* with electrons as the majority carriers, and (2) *P-Channel JFET* with holes as the majority carriers.

7.2 CONSTRUCTION OF N-CHANNEL JFET

It consists of a N-type bar which is made of silicon. Ohmic contacts (terminals), made at the two ends of the bar, are called Source and Drain.

Source (S) This terminal is connected to the negative pole of the battery. Electrons which are the majority carriers in the N-type bar enter the bar through this terminal.

Drain (D) This terminal is connected to the positive pole of the battery. The majority carriers leave the bar through this terminal.

Gate (G) Heavily doped P-type silicon is diffused on both sides of the N-type silicon bar by which PN junctions are formed. These layers are joined together and called Gate *G*.

Channel The region *BC* of the N-type bar between the depletion region is called the channel. Majority carriers move from the source to drain when a potential difference V_{DS} is applied between the source and drain.

7.3 OPERATION OF N-CHANNEL JFET

When $V_{GS} = 0$ and $V_{DS} = 0$ When no voltage is applied between drain and source, and gate and source, the thickness of the depletion regions round the PN junction is uniform as shown in Fig. 7.1.

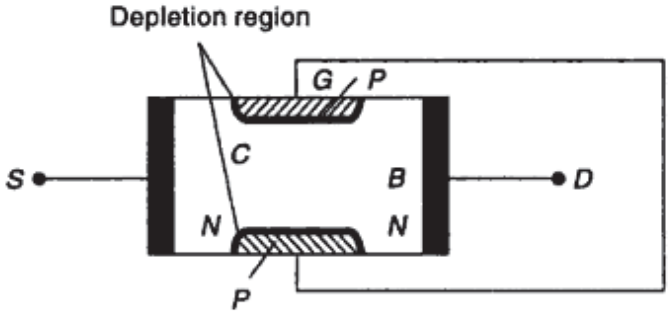

Fig. 7.1 JFET construction

When $V_{DS} = 0$ and V_{GS} is decreased from zero In this case, the PN junctions are reverse biased and hence the thickness of the depletion region increases. As V_{GS} is decreased from zero, the reverse bias voltage across the PN junction is increased and hence, the thickness of the depletion region in the channel until the two depletion regions make contact with each other. In this condition, the channel is said to be cut-off. The value of V_{GS} which is required to cut-off the channel is called the cut-off voltage V_C.

When $V_{GS} = 0$ and V_{DS} is increased from zero Drain is positive with respect to the source with $V_{GS} = 0$. Now the majority carriers (electrons) flow through the N-channel from source to drain. Therefore the conventional current I_D flows from drain to source. The magnitude of the current will depend upon the following factors:

1. The number of majority carriers (electrons) available in the channel, i.e. the conductivity of the channel.
2. The length L of the channel.
3. The cross-sectional area A of the channel at B.
4. The magnitude of the applied voltage V_{DS}. Thus the channel acts as a resistor of resistance R given by

$$R = \frac{\rho L}{A} \tag{7.1}$$

$$I_D = \frac{V_{DS}}{R} = \frac{AV_{DS}}{\rho L} \tag{7.2}$$

where ρ is the resistivity of the channel. Because of the resistance of the channel and the applied voltage V_{DS}, there is a gradual increase of positive potential along the channel from source to drain. Thus the reverse voltage across the PN junctions increases and hence the thickness of the depletion regions also increases. Therefore, the channel is wedge shaped as shown in Fig. 7.2.

As V_{DS} is increased, the cross-sectional area of the channel will be reduced. At a certain value V_P of V_{DS}, the cross-sectional area at B becomes minimum. At this voltage, the channel is said to be pinched off and the drain voltage V_P is called the pinch-off voltage.

As a result of the decreasing cross-section of the channel with the increase of V_{DS}, the following results are obtained.

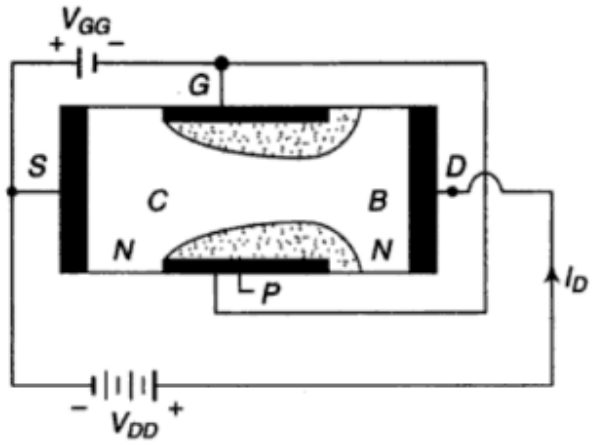

Fig. 7.2 JFET under applied bias

(i) As V_{DS} is increased from zero, I_D increases along OP, and the rate of increase of I_D with V_{DS} decreases as shown in Fig. 7.3. The region from $V_{DS} = 0$V to $V_{DS} = V_P$ is called the ohmic region. In the channel ohmic region the drain to source resistance $\frac{V_{DS}}{I_D}$ is related to the gate voltage V_{GS}, in an almost linear manner. This is useful as a voltage variable resistor (VVR) or voltage dependent resistor (VDR).

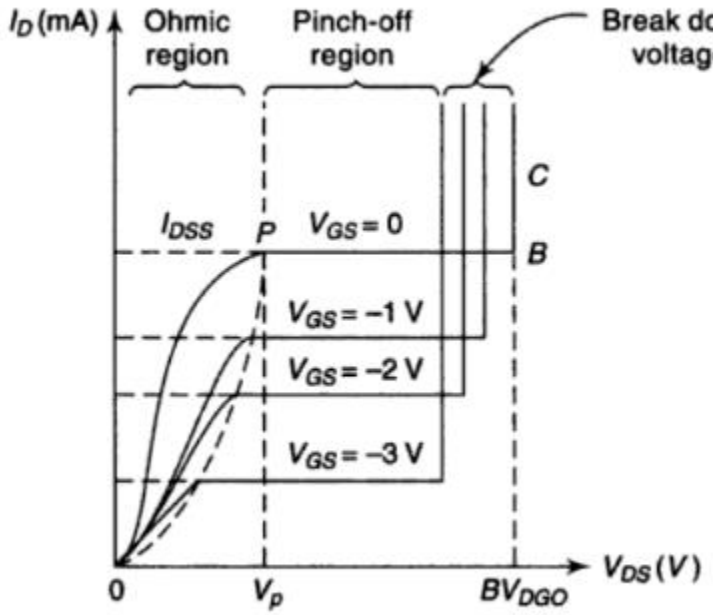

Fig. 7.3 Drain characteristics

(ii) When $V_{DS} = V_P$, I_D becomes maximum. When V_{DS} is increased beyond V_P, the length of the pinch-off or saturation region increases. Hence, there is no further increase of I_D.

(iii) At a certain voltage corresponding to the point B, I_D suddenly increases. This effect is due to the Avalanche multiplication of electrons caused by breaking of covalent bonds of silicon atoms in the depletion region between the gate and the drain. The drain voltage at which the breakdown occurs is denoted by BV_{DGO}. The variation of I_D with V_{DS} when $V_{GS} = 0$ is shown in Fig. 7.3 by the curve *OPBC*.

When V_{GS} is negative and V_{DS} is increased When the gate is maintained at a negative voltage less than the negative cut-off voltage, the reverse voltage across

the junction is further increased. Hence for a negative value of V_{GS}, the curve of I_D versus V_{DS} is similar to that for $V_{GS} = 0$, but the values of V_P and BV_{DGO} are lower, as shown in Fig. 7.3.

From the curves, it is seen that above the pinch-off voltage, at a constant value of V_{DS}, I_D increases with an increase of V_{GS}. Hence, a JFET is suitable for use as a voltage amplifier, similar to a transistor amplifier.

It can be seen from the curve that for voltage $V_{DS} = V_P$, the drain current is not reduced to zero. If the drain current is to be reduced to zero, the ohmic voltage drop along the channel should also be reduced to zero. Further, the reverse biasing to the gate-source PN junction essential for pinching off the channel would also be absent.

The drain current I_D is controlled by the electric field that extends into the channel due to reverse biased voltage applied to the gate; hence, this device has been given the name *Field Effect Transistor*.

In a bar of P-type semiconductor, the gate is formed due to N-type semiconductor. The working of the P-channel JFET will be similar to that of N-channel JFET with proper alterations in the biasing circuits; in this case holes will be the current carriers instead of electrons. The circuit symbols for N-channel and P-channel JFETs are shown in Fig. 7.4. It should be noted that the direction of the arrow points in the direction of conventional current which would flow into the gate if the PN junction was forward biased.

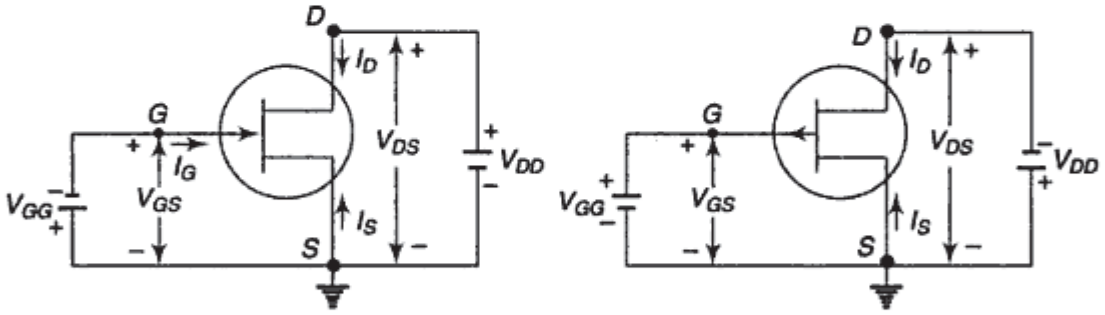

Fig. 7.4 Circuit symbols for N- and P-channel JFET

7.4 CHARACTERISTIC PARAMETERS OF THE JFET

In a JFET, the drain current I_D depends upon the drain voltage V_{DS} and the gate voltage V_{GS}. Any one of these variables may be fixed and the relation between the other two are determined. These relations are determined by the three parameters which are defined below.

(1) Mutual conductance or transconductance, g_m It is the slope of the transfer characteristic curves, and is defined by

$$g_m = \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}} = \frac{\Delta I_D}{\Delta V_{GS}}, V_{DS} \text{ held constant.}$$

It is the ratio of a small change in the drain current to the corresponding small change in the gate voltage at a constant drain voltage. The change in I_D and V_{GS}

should be taken on the straight part of the transfer characteristics. It has the unit of conductance in mho.

(2) Drain resistance, r_d It is the reciprocal of the slope of the drain characteristics and is defined by

$$r_d = \left(\frac{\partial V_{DS}}{\partial I_D}\right)_{V_{GS}} = \frac{\Delta V_{DS}}{\Delta I_D}, V_{GS} \text{ held constant.}$$

It is the ratio of a small change in the drain voltage to the corresponding small change in the drain current at a constant gate voltage. It has the unit of resistance in ohms.

The drain resistance at $V_{GS} = 0$ V, i.e. when the depletion regions of the channel are absent, is called as *drain-source ON resistance,* represented as R_{DS} or $R_{DS(ON)}$.

The reciprocal of r_d is called the drain conductance. It is denoted by g_d or g_{os}.

(3) Amplification factor, μ It is defined by

$$\mu = -\left(\frac{\partial V_{DS}}{\partial V_{GS}}\right) I_D = -\frac{\Delta V_{DS}}{\Delta V_{GS}}, I_D \text{ held constant.}$$

It is the ratio of a small change in the drain voltage to the corresponding small change in the gate voltage at a constant drain current. Here, the negative sign shows that when V_{GS} is increased, V_{DS} must be decreased for I_D to remain constant.

(4) Relationship among FET parameters As I_D depends on V_{DS} and V_{GS}, the functional equation can be expressed as

$$I_D = f(V_{DS}, V_{GS})$$

If the drain voltage is changed by a small amount from V_{DS} to $(V_{DS} + \Delta V_{DS})$ and the gate voltage is changed by a small amount from V_{GS} to $(V_{GS} + \Delta V_{GS})$, then the corresponding small change in I_D may be obtained by applying Taylor's theorem with neglecting higher order terms. Thus the small change ΔI_D is given by

$$\Delta I_D = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} \Delta V_{DS} + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}} \Delta V_{GS}$$

Dividing both the sides of this equation by ΔV_{GS}, we obtain

$$\frac{\Delta I_D}{\Delta V_{GS}} = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} \left(\frac{\Delta V_{DS}}{\Delta V_{GS}}\right) + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}}$$

If I_D is constant, then $\frac{\Delta I_D}{\Delta V_{GS}} = 0$

Therefore, we have

$$0 = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} \left(\frac{\Delta V_{DS}}{\Delta V_{GS}}\right)_{I_D} + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}}$$

Substituting the values of the partial differential coefficients, we get

$$0 = \left(\frac{1}{r_d}\right)(-\mu) + g_m$$

Hence, $\mu = r_d \, X \, g_m$

Therefore, amplification factor (μ) is the product of drain resistance (r_d) and transconductance (g_m).

(5) Power dissipation, P_D The FET's continuous power dissipation, P_D, is the product of I_D and V_{DS}.

Example 7.1 When a reverse gate voltage of 12 V is applied to JFET, the gate current is 1 nA. Determine the resistance between gate and source.

Solution: $V_{GS} = 12$ V, $I_G = 10^{-9}$ A.

Therefore, gate-to-source resistance $= \dfrac{V_{GS}}{I_G} = \dfrac{12}{10^{-9}} = 12{,}000 \text{ M}\Omega$

Example 7.2 When the reverse gate voltage of JFET changes from 4.0 to 3.9 V, the drain current changes from 1.3 to 1.6 mA. Find the value of transconductance.

Solution: $\Delta V_{GS} = 4.0 - 3.9 = 0.1$ V

$\Delta I_D = 1.6 - 1.3 = 0.3$ mA

Therefore, transconductance, $g_m = \dfrac{\Delta I_D}{\Delta V_{GS}} = \dfrac{0.3 \times 10^{-3}}{0.1} = 3$ m mho.

Example 7.3 A FET has a driven current of 4 mA. If D_{SS} = 8 mA and $V_{GS(off)}$ = –6 V. Find the values of V_{GS} and V_P.

Solution:

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$

$$4 = 8\left[1 + \frac{V_{GS}}{6}\right]^2$$

$$1 + \frac{V_{GS}}{6} = \sqrt{\frac{4}{8}} = \frac{1}{\sqrt{2}} = 0.707$$

Therefore, $V_{GS} = -1.76$ V

$V_P = |V_{GS(off)}| = 6$V

7.5 EXPRESSION FOR SATURATION DRAIN CURRENT

For the transfer characteristics, V_{DS} is maintained constant at a suitable value greater than the pinch-off voltage V_P. The gate voltage V_{GS} is decreased from zero till I_D is reduced to zero. The transfer characteristics I_D versus V_{GS} is shown in Fig. 7.5. The

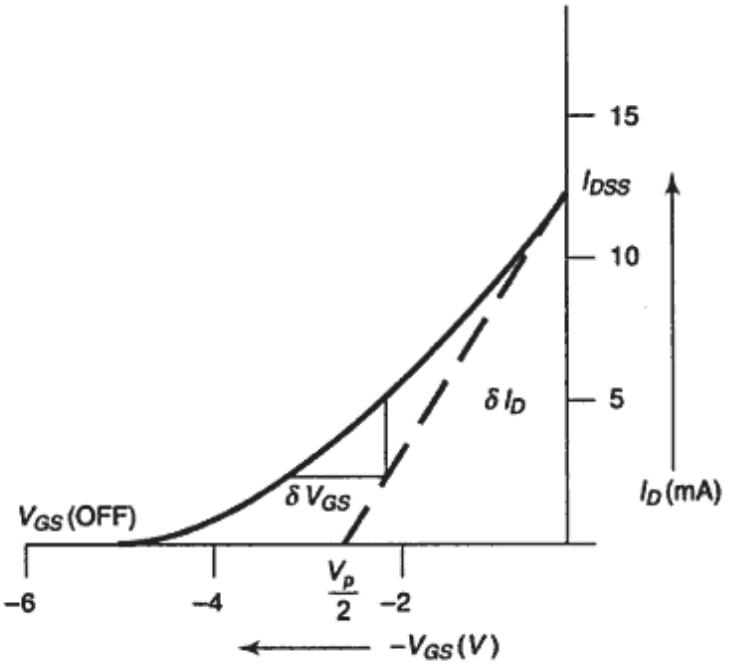

Fig. 7.5 Transfer characteristics of JFET

shape of the transfer characteristic is very nearly a parabola. It is found that the characteristic is approximately represented by the parabola,

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \tag{7.3}$$

where I_{DS} is the saturation drain current, I_{DSS} is the value of I_{DS} when $V_{GS} = 0$, and V_P is the pinch-off voltage.

Differentiating Eq. (7.3) with respect to V_{GS} we can obtain an expression for g_m.

$$\frac{\partial I_{DS}}{\partial V_{GS}} = I_{DSS} \times 2\left(1 - \frac{V_{GS}}{V_P}\right)\left(-\frac{1}{V_P}\right)$$

We know that $g_m = \dfrac{\delta I_{DS}}{\delta V_{GS}}$, V_{DS} is constant.

Therefore, $g_m = \dfrac{-2\,I_{DSS}}{V_P}\left(1 - \dfrac{V_{GS}}{V_P}\right)$ (7.4)

Now from Eqn. (7.3), we have

$$\left(1 - \frac{V_{GS}}{V_P}\right) = \sqrt{\frac{I_{DS}}{I_{DSS}}} \tag{7.5}$$

Substituting this value in Eqn. (7.4), we get

$$g_m = \frac{-2\sqrt{I_{DS}\ I_{DSS}}}{V_P}$$

Suppose $g_m = g_{mo}$, when $V_{GS} = 0$, then from Eqn. (7.4)

$$g_{mo} = -\frac{2I_{DSS}}{V_P} \tag{7.6}$$

Therefore, from Eqs (7.4) and (7.6)

$$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right) \tag{7.7}$$

Equation (7.5) shows that g_m varies as the square root of the saturation drain current I_{DS}, and Eqn. (7.7) shows that g_m decreases linearly with increase of V_{GS}.

7.6 SLOPE OF THE TRANSFER CHARACTERISTIC AT I_{DSS}

From Eq. (7.5), we have

$$g_m = \frac{2\sqrt{I_{DS}\ I_{DSS}}}{V_P}$$

or

$$\frac{\partial I_{DS}}{\partial V_{GS}} = \frac{2\sqrt{I_{DS}\ I_{DSS}}}{V_P}$$

Substituting $I_{DS} = I_{DSS}$,

$$\frac{\partial I_{DS}}{\partial V_{GS}} = -\frac{2I_{DSS}}{V_P} = \frac{I_{DSS}}{\frac{-V_P}{2}}$$

This equation shows that the tangent to the curve at $I_{DS} = I_{DSS}$, $V_{GS} = 0$, will have an intercept at $\frac{-V_P}{2}$ on the axis of V_{GS} as shown in Fig. 7.5. Therefore, the value of V_P can be found by drawing the tangent at $I_{DS} = I_{DSS}$, $V_{GS} = 0$.

The gate-source cut off voltage, $V_{GS(off)}$, on the transfer characteristic is equal to the pinch off voltage, V_P, on the drain characteristics, i.e. $V_P = |V_{GS(off)}|$.

Therefore, $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$

Example 7.4 An N-channel JFET has $I_{DSS} = 8$ mA and $V_p = -5$ V. Determine the minimum value of V_{DS} for pinch-off region and the drain current I_{DS}, for $V_{GS} = -2$ V in the pinch-off region.

Solution: The minimum value of V_{DS} for pinch-off to occur for $V_{GS} = -2$ V is

$$V_{DSmin} = V_{GS} - V_P = -2 - (-5) = 3\text{V}$$

$$I_{DS} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$= 8 \times 10^{-3}\,[1 - (-2)/(-5)]^2 = 2.88\ \text{mA}$$

7.7 COMPARISON OF JFET AND BJT

1. FET operation depends only on the flow of majority carriers-holes for P-channel FETs and electrons for N-channel FETs. Therefore, they are called Unipolar devices. Bipolar transistor (BJT) operation depends on both minority and majority current carriers.
2. As FET has no junctions and the conduction is through an N-type or P-type semiconductor material, FET is less noisy than BJT.
3. As the input circuit of FET is reverse biased, FET exhibits a much higher input impedance (in the order of 100 M Ω) and lower output impedance and there will be a high degree of isolation between input and output. So, FET can act as an excellent buffer amplifier but the BJT has low input impedance because its input circuit is forward biased.
4. FET is a voltage controlled device, i.e. voltage at the input terminal controls the output current, whereas BJT is a current controlled device, i.e. the input current controls the output current.
5. FETs are much easier to fabricate and are particularly suitable for ICs because they occupy less space than BJTs.
6. The performance of BJT is degraded by neutron radiation because of the reduction in minority-carrier lifetime, whereas FET can tolerate a much higher level of radiation since they do not rely on minority carriers for their operation.
7. The performance of FET is relatively unaffected by ambient temperature changes. As it has a negative temperature coefficient at high current levels, it prevents the FET from thermal breakdown. The BJT has a positive temperature coefficient at high current levels which leads to thermal breakdown.
8. Since FET does not suffer from minority carrier storage effects, it has higher switching speeds and cut-off frequencies. BJT suffers from minority carrier storage effects and therefore has lower switching speed and cut-off frequencies.
9. FET amplifiers have low gain bandwidth product due to the junction capacitive effects and produce more signal distortion except for small signal operation.
10. BJTs are cheaper to produce than FETs.

7.8 APPLICATIONS OF JFET

1. FET is used as a buffer in measuring instruments, receivers since it has high input impedance and low output impedance.
2. FETs are used in RF amplifiers in FM tuners and communication equipment for the low noise level.
3. Since the input capacitance is low, FETs are used in cascade amplifiers in measuring and test equipments.
4. Since the device is voltage controlled, it is used as a voltage variable resistor in operational amplifiers and tone controls.
5. FETs are used in mixer circuits in FM and TV receivers, and communication equipment because inter modulation distortion is low.
6. It is used in oscillator circuits because frequency drift is low.
7. As the coupling capacitor is small, FETs are used in low frequency amplifiers in hearing aids and inductive transducers.