# 6 Bipolar Junction Transistor

## 6.1 INTRODUCTION

A Bipolar Junction Transistor (BJT) is a three terminal semiconductor device in which the operation depends on the interaction of both majority and minority carriers and hence the name Bipolar. The BJT is analogous to a vacuum triode and is comparatively smaller in size. It is used in amplifier and oscillator circuits, and as a switch in digital circuits. It has wide applications in computers, satellites and other modern communication systems.

## 6.2 CONSTRUCTION

The BJT consists of a silicon (or germanium) crystal in which a thin layer of N-type Silicon is sandwiched between two layers of P-type silicon. This transistor is referred to as PNP. Alternatively, in a NPN transistor, a layer of P-type material is sandwiched between two layers of N-type material. The two types of the BJT are represented in Fig. 6.1.

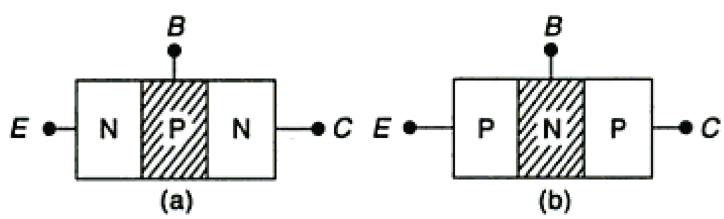


**Fig. 6.1** Transistor (a) NPN and (b) PNP

The symbolic representation of the two types of the BJT is shown in Fig. 6.2. The three portions of the transistor are Emitter, Base and Collector, shown as *E*, *B* and *C*, respectively. The arrow on the emitter specifies the direction of current flow when the *EB* junction is forward biased.

Emitter is heavily doped so that it can inject a large number of charge carriers into the base. Base is lightly doped and very thin. It passes most of the injected charge carriers from the emitter into the collector. Collector is moderately doped.

## 6.3 TRANSISTOR BIASING

As shown in Fig. 6.3, usually the emitter-base junction is forward biased and collector-base junction is reverse biased. Due to the forward bias on the emitter-base

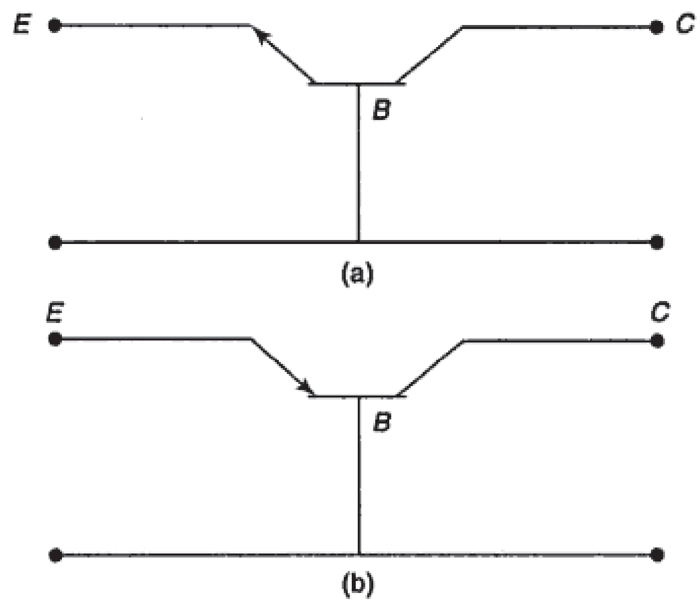


**Fig. 6.2** Circuit symbol. (a) NPN transistor and (b) PNP transistor

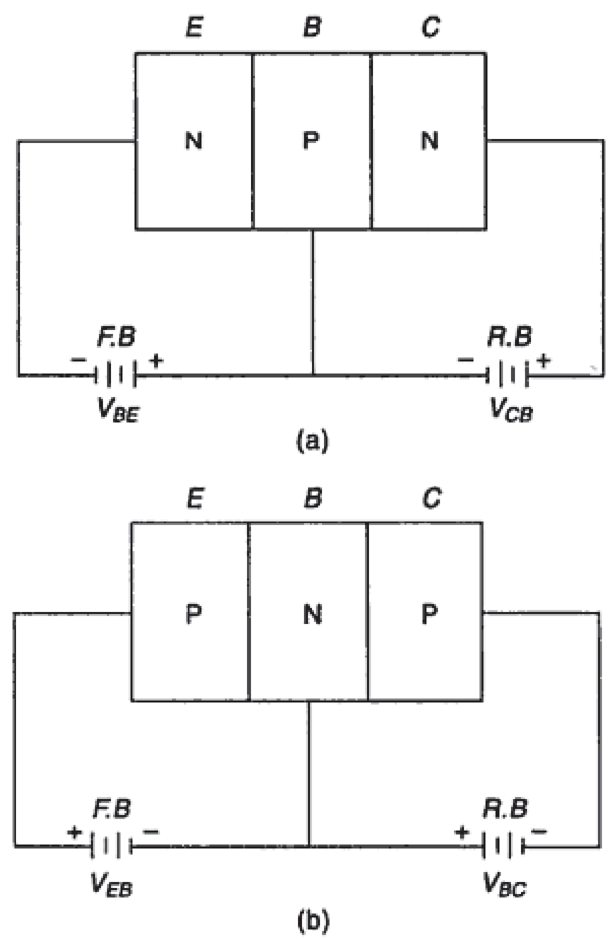


**Fig. 6.3** Transistor biasing (a) NPN transistor and (b) PNP transistor

junction an emitter current flows through the base into the collector. Though the, collector-base junction is reverse biased, almost the entire emitter current flows through the collector circuit.

## 6.4 OPERATION OF NPN TRANSISTOR

As shown in Fig. 6.4, the forward bias applied to the emitter base junction of an NPN transistor causes a lot of electrons from the emitter region to crossover to the base region. As the base is lightly doped with P-type impurity, the number of holes in the base region is very small and hence the number of electrons that combine with holes in the P-type base region is also very small. Hence a few electrons combine with holes to constitute a base current $I_B$. The remaining electrons (more than 95%) crossover into the collector region to constitute a collector current $I_C$. Thus the base and collector current summed up gives the emitter current, i.e. $I_E = -(I_C + I_B)$.

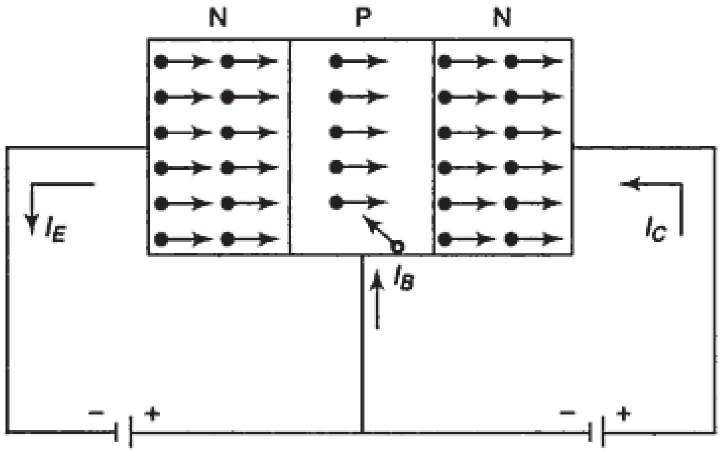


**Fig. 6.4** Current in NPN transistor

In the external circuit of the NPN bipolar junction transistor, the magnitudes of the emitter current $I_E$, the base current $I_B$ and the collector current $I_C$ are related by $I_E = I_C + I_B$.

## 6.5 OPERATION OF PNP TRANSISTOR

As shown in Fig. 6.5, the forward bias applied to the emitter-base junction of a PNP transistor causes a lot of holes from the emitter region to crossover to the base region as the base is lightly doped with N-types impurity. The number of electrons in the base region is very small and hence the number of holes combined with

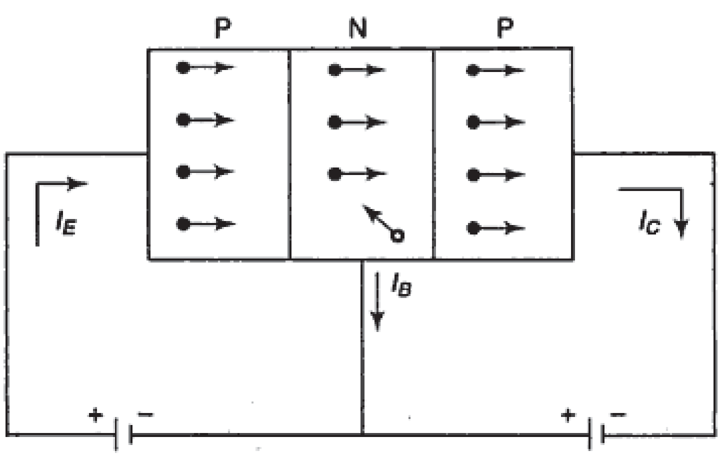


**Fig. 6.5** Current in PNP transistor

electrons in the N-type base region is also very small. Hence a few holes combined with electrons to constitute a base current $I_B$. The remaining holes (more than 95%) crossover into the collector region to constitute a collector current $I_C$. Thus the collector and base current when summed up gives the emitter current, i.e. $I_E = -(I_C + I_B)$.

In the external circuit of the PNP bipolar junction transistor, the magnitudes of the emitter current $I_E$, the base current $I_B$ and the collector current $I_C$ are related by

$$I_E = I_C + I_B \tag{6.1}$$

This equation gives the fundamental relationship between the currents in a bipolar transistor circuit. Also, this fundamental equation shows that there are current amplification factors $\alpha$ and $\beta$ in common base transistor configuration and common emitter transistor configuration respectively for the static (d.c.) currents, and for small changes in the currents.

*Large-signal current gain($\alpha$)* The large signal current gain of a common base transistor is defined as the ratio of the negative of the collector-current increment to the emitter-current change from cutoff ($I_E = 0$) to $I_E$, i.e.

$$\alpha = -\frac{(I_c - I_{CBO})}{I_E - 0}$$

where $I_{CBO}$ (or $I_{CO}$) is the reverse saturation current flowing through the reverse biased collector-base junction, i.e. the collector to base leakage current with emitter open. As the magnitude of $I_{CBO}$ is negligible when compared to $I_E$, the above expression can be written as

$$\alpha = \frac{I_C}{I_E} \tag{6.3}$$

Since $I_C$ and $I_E$ are flowing in opposite directions, $\alpha$ is always positive. Typical value of $\alpha$ ranges from 0.90 to 0.995. Also, $\alpha$ is not a constant but varies with emitter current $I_E$, collector voltage $V_{CB}$ and temperature.

**General Transistor Equation**

In the active region of the transistor, the emitter is forward biased and the collector is reverse biased. The generalised expression for collector current $I_C$ for collector junction voltage $V_C$ and emitter current $I_E$ is given by

$$I_C = -\alpha I_E + I_{CBO}(1 - e^{V_c/V_T}) \tag{6.4}$$

If $V_C$ is negative and $|V_c|$ is very large compared with $V_T$, then the above equation reduces to

$$I_C = -\alpha I_E + I_{CBO} \tag{6.5}$$

If $V_C$, i.e. $V_{CB}$, is few volts, $I_C$ is independent of $V_C$. Hence the collector current $I_C$ is determined only by the fraction $\alpha$ of the current $I_E$ flowing in the emitter.

*Relation among $I_C$, $I_B$ and $I_{CBO}$* From Eqn. (6.5), We have

$$I_C = -\alpha I_E + I_{CBO}$$

Since $I_C$ and $I_E$ are flowing in opposite directions,

$$I_E = -(I_C + I_B)$$

Therefore, $I_C = -\alpha[-(I_C + I_B)] + I_{CBO}$

$$I_C - \alpha I_C = \alpha I_B + I_{CBO}$$

$$I_C(1-\alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{CBO}}{1-\alpha}$$

Since $\beta = \frac{\alpha}{1-\alpha}$, (6.6)

the above expression becomes

$$I_C = (1+\beta) I_{CBO} + \beta I_B \quad (6.7)$$

*Relation among $I_C$, $I_B$ and $I_{CEO}$* In the common-emitter (CE) transistor circuit, $I_B$ is the input current and $I_C$ is the output current. If the base circuit is open, i.e, $I_B = 0$, then a small collector current flows from the collector to emitter. This is denoted as $I_{CEO}$, the collector-emitter current with base open. This current $I_{CEO}$ is also called the collector to emitter leakage current.

In this CE configuration of the transistor, the emitter-base junction is forward-biased and collector-base junction is reverse-biased and hence the collector current $I_C$ is the sum of the part of the emitter current $I_E$ that reaches the collector, and the collector-emitter leakage current $I_{CEO}$. Therefore, the part of $I_E$, which reaches collector is equal to $(I_C - I_{CEO})$.

Hence, the *large-signal current gain* ($\beta$) is defined as,

$$\beta = \frac{(I_C - I_{CEO})}{I_B} \quad (6.8)$$

From the equation, we have

$$I_C = \beta I_B + I_{CEO} \quad (6.9)$$

*Relation between $I_{CBO}$ and $I_{CEO}$* Comparing Eqs. (6.7) and (6.9), we get the relationship between the leakage currents of transistor common-base (CB) and common-emitter (CE) configurations as

$$I_{CEO} = (1+\beta) I_{CBO} \quad (6.10)$$

From this equation, it is evident that the collector-emitter leakage current ($I_{CEO}$) in CE configuration is $(1+\beta)$ times larger than that in CB configuration. As $I_{CBO}$ is temperature-dependent, $I_{CEO}$ varies by large amount when temperature of the junctions changes.

**Expression for Emitter Current**

The magnitude of emitter-current is

$$I_E = I_C + I_B$$

Substituting Eqn. (6.7) in the above equation, we get

$$I_E = (1+\beta) I_{CBO} + (1+\beta) I_B \quad (6.11)$$

Substituting Eqn. (6.6) into Eqn. (6.11), we have

$$I_E = \frac{1}{1-\alpha} I_{CBO} + \frac{1}{1-\alpha} I_B \quad (6.12)$$

*DC current gain ($\beta_{d.c.}$ or $h_{FE}$)* The d.c. current gain is defined as the ratio of the collector current $I_C$ to the base current $I_B$. That is,

$$\beta_{\text{d.c.}} = h_{FE} = \frac{I_C}{I_B} \tag{6.13}$$

As $I_C$ is large compared with $I_{CEO}$, the large signal current gain ($\beta$) and the d.c. current gain ($h_{FE}$) are approximately equal.

## 6.6 TYPES OF CONFIGURATION

When a transistor is to be connected in a circuit, one terminal is used as an input terminal, the other terminal is used as an output terminal and the third terminal is common to the input and output. Depending upon the input, output and common terminal, a transistor can be connected in three configurations. They are: (i) Common base (CB) configuration, (ii) Common emitter (CE) configuration, and (iii) Common collector (CC) configuration.

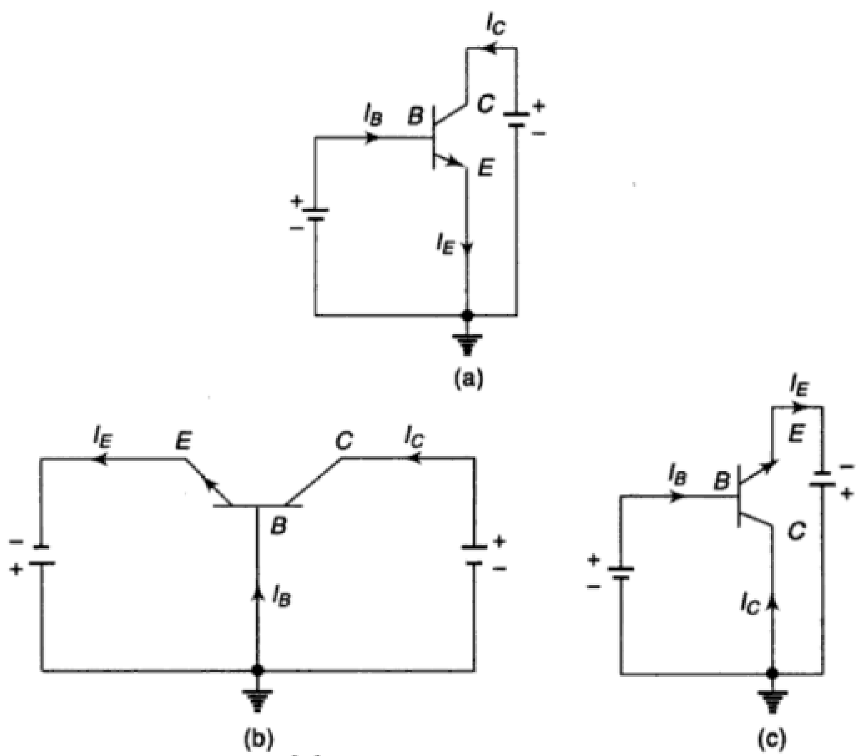


**Fig. 6.6** Transistor configuration: (a) common base (b) common emitter and (c) common collector

*(i) CB configuration* This is also called grounded base configuration. In this configuration, emitter is the input terminal, collector is the output terminal and base is the common terminal.

*(ii) CE configuration* This is also called grounded emitter configuration. In this configuration, base is the input terminal, collector is the output terminal and emitter is the common terminal.

*(iii) CC configuration* This is also called grounded collector configuration. In this configuration, base is the input terminal, emitter is the output terminal and collector is the common terminal.

The supply voltage connections for normal operation of an NPN transistor in the three configurations are shown in Fig. 6.6.

### 6.6.1 CB Configuration

The circuit diagram for determining the static characteristics curves of an NPN transistor in the common base configuration is shown in Fig. 6.7.

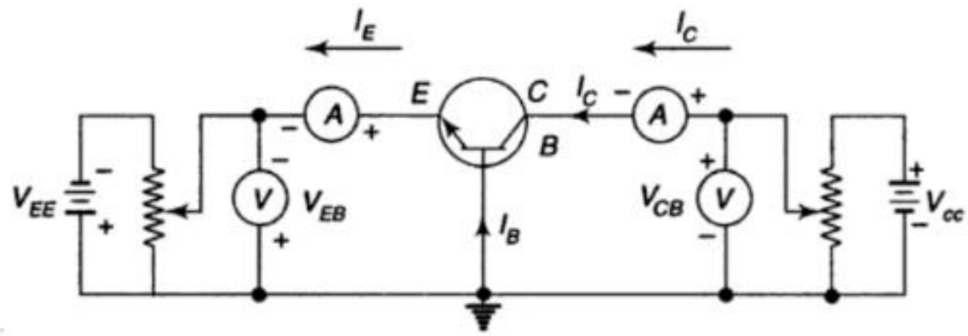


**Fig. 6.7** Circuit to determine CB static characteristics

*Input characteristics* To determine the input characteristics, the collector-base voltage $V_{CB}$ is kept constant at zero volt and the emitter current $I_E$ is increased from zero in suitable equal steps by increasing $V_{EB}$. This is repeated for higher fixed values of $V_{CB}$. A curve is drawn between emitter current $I_E$ and emitter-base voltage $V_{EB}$ at constant collector-base voltage $V_{CB}$. The input characteristics thus obtained are shown in Fig. 6.8.

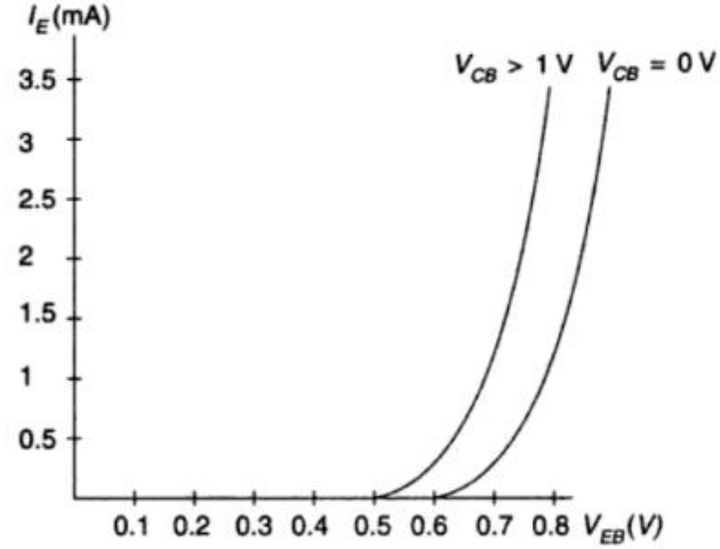


**Fig. 6.8** CB input characteristics

When $V_{CB}$ is equal to zero and the emitter-base junction is forward biased as shown in the characteristics, the junction behaves as a forward biased diode so that emitter current $I_E$ increases rapidly with small increase in emitter-base voltage $V_{EB}$. When $V_{CB}$ is increased keeping $V_{EB}$ constant, the width of the base region will decrease. This effect results in an increase of $I_E$. Therefore, the curves shift towards the left as $V_{CB}$ is increased.

*Output characteristics* To determine the output characteristics, the emitter current $I_E$ is kept constant at a suitable value by adjusting the emitter-base voltage $V_{EB}$. Then $V_{CB}$ is increased in suitable equal steps and the collector current $I_C$ is noted for each value of $I_E$. This is repeated for different fixed values of $I_E$. Now the curves of $I_C$ versus $V_{CB}$ are plotted for constant values of $I_E$ and the output characteristics thus obtained is shown in Fig. 6.9.

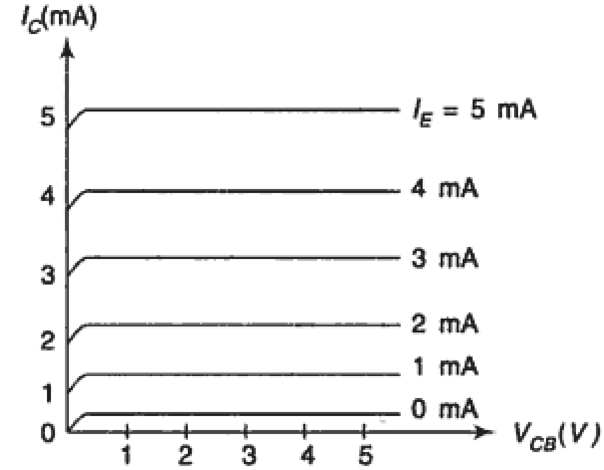


**Fig. 6.9** CB output characteristics

From the characteristics, it is seen that for a constant value of $I_E$, $I_C$ is independent of $V_{CB}$ and the curves are parallel to the axis of $V_{CB}$. Further, $I_C$ flows even when $V_{CB}$ is equal to zero. As the emitter-base junction is forward biased, the majority carriers, i.e. electrons, from the emitter are injected into the base region. Due to the action of the internal potential barrier at the reverse biased collector-base junction, they flow to the collector region and give rise to $I_C$ even when $V_{CB}$ is equal to zero.

*Early effect or base-width modulation* As the collector voltage $V_{CC}$ is made to increase the reverse bias, the space charge width between collector and base tends to increase, with the result that the effective width of the base decreases. This dependency of base-width on collector-to-emitter voltage is known as the *Early effect*. This decrease in effective base-width has three consequences:

(i) There is less chance for recombination within the base region. Hence, $\alpha$ increases with increasing $|V_{CB}|$.

(ii) The charge gradient is increased within the base, and consequently, the current of minority carriers injected across the emitter junction increases.

(iii) For extremely large voltages, the effective base-width may be reduced to zero, causing voltage breakdown in the transistor. This phenomenon is called the *punch through*.

For higher values of $V_{CB}$, due to Early effect, the value of $\alpha$ increases. For example, $\alpha$ changes, say from 0.98 to 0.985. Hence, there is a very small positive slope in the CB output characteristics and hence the output resistance is not zero.

*Transistor parameters* The slope of the CB characteristics will give the following four transistor parameters. Since these parameters have different dimensions, they are commonly known as common base *hybrid parameters* or *h-parameters*.

*(i) Input impedance ($h_{ib}$):* It is defined as the ratio of the change in (input) emitter voltage to the change in (input) emitter current with the (output) collector voltage $V_{CB}$ kept constant. Therefore,

$$h_{ib} = \frac{\Delta V_{EB}}{\Delta I_E}, V_{CB} \text{ constant} \quad (6.14)$$

It is the slope of CB input characteristics $I_E$ versus $V_{EB}$ as shown in Fig. 6.8. The typical value of $h_{ib}$ ranges from 20Ω to 50Ω.

*(ii) Output admittance ($h_{ob}$)*: It is defined as the ratio of change in the (output) collector current to the corresponding change in the (output) collector voltage with the (input) emitter current $I_E$ kept constant. Therefore,

$$h_{ob} = \frac{\Delta I_C}{\Delta V_{CB}}, I_E \text{ constant} \quad (6.15)$$

It is the slope of CB output characteristics $I_C$ versus $V_{CB}$ as shown in Fig. 6.9. The typical value of this parameter is of the order of 0.1 to 10 μ mhos.

*(iii) Forward current gain ($h_{fb}$)*: It is defined as a ratio of the change in the (output) collector current to the corresponding change in the (input) emitter current keeping the (output) collector voltage $V_{CB}$ constant. Hence,

$$h_{fb} = \frac{\Delta I_C}{\Delta I_E}, V_{CB} \text{ constant.} \quad (6.16)$$

It is the slope of $I_C$ versus $I_E$ curve. Its typical value varies from 0.9 to 1.0.

*(iv) Reverse voltage gain ($h_{rb}$)*: It is defined as the ratio of the change in the (input) emitter voltage and the corresponding change in (output) collector voltage with constant (input) emitter current, $I_E$. Hence,

$$h_{rb} = \frac{\Delta V_{EB}}{\Delta V_{CB}}, I_E \text{ constants} \quad (6.17)$$

It is the slope of $V_{EB}$ versus $V_{CB}$ curve. Its typical value is of the order of $10^{-5}$ to $10^{-4}$.

### 6.6.2 CE Configuration

*Input characteristics* To determine the input characteristics, the collector to emitter voltage is kept constant at zero volt and base current is increased from zero in equal steps by increasing $V_{BE}$ in the circuit shown in Fig. 6.10.

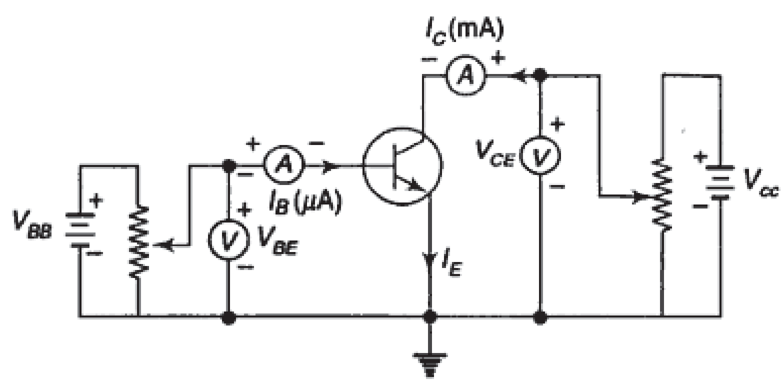


**Fig. 6.10** Circuit to determine CE static characteristics

The value of $V_{BE}$ is noted for each setting of $I_B$. This procedure is repeated for higher fixed values of $V_{CE}$, and the curves of $I_B$ $V_s$. $V_{BE}$ are drawn. The input characteristics thus obtained are shown in Fig. 6.11.

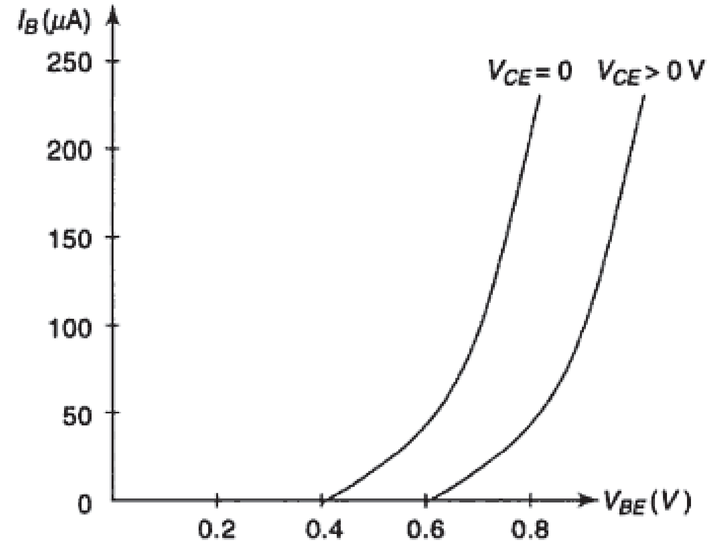


**Fig. 6.11** CE input characteristics

When $V_{CE}$ = 0, the emitter-base junction is forward biased and the junction behaves as a forward biased diode. Hence the input characteristic for $V_{CE}$ = 0 is similar to that of a forward-biased diode. When $V_{CE}$ is increased, the width of the depletion region at the reverse biased collector-base junction will increase. Hence the effective width of the base will decrease. This effect causes a decrease in the base current $I_B$. Hence, to get the same value of $I_b$ as that for $V_{CE} = 0$, $V_{BE}$ should be increased. Therefore, the curve shifts to the right as $V_{CE}$ increases.

*Output characteristics* To determine the output characteristics, the base current $I_B$ is kept constant at a suitable value by adjusting base-emitter voltage, $V_{BE}$. The magnitude of collector-emitter voltage $V_{CE}$ is increased in suitable equal steps from zero and the collector current $I_C$ is noted for each setting $V_{CE}$. Now the curves of $I_C$ versus $V_{CE}$ are plotted for different constant values of $I_B$. The output characteristics thus obtained are shown in Fig. 6.12. From Eqs. (6.6) and (6.7), we have

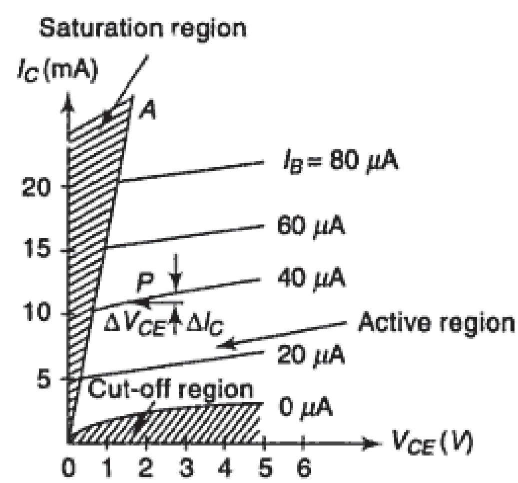


**Fig. 6.12** CE output characteristics

$$\beta = \frac{\alpha}{1-\alpha} \quad \text{and} \quad I_C = (1+\beta)\, I_{CBO} + \beta I_B$$

For larger values of $V_{CE}$, due to Early effect, a very small change in $\alpha$ is reflected in a very large change in $\beta$. For example, when $\alpha$ = 0.98, $\beta = \frac{0.98}{1-0.98} = 49$. If $\alpha$ increases to 0.985, then $\beta = \frac{0.985}{1-0.985} = 66$. Here, a slight increase in $\alpha$ by about 0.5% results in an increases in $\beta$ by about 34%. Hence, the output characteristics of CE configuration show a larger slope when compared with CB configuration.

The output characteristics have three regions, namely, saturation region, cutoff region and active region. The region of curves to the left of the line *OA* is called the *saturation region* (hatched), and the line *OA* is called the saturation line. In this region, both junctions are forward biased and an increase in the base current does not cause a corresponding large change in $I_C$. The ratio of $V_{CE(sat)}$ to $I_C$ in this region is called saturation resistance.

The region below the curve for $I_B = 0$ is called the *cut-off region* (hatched). In this region, both junctions are reverse biased. When the operating point for the transistor enters the cut-off region, the transistor is OFF. Hence, the collector current becomes almost zero and the collector voltage almost equals $V_{CC}$, the collector supply voltage. The transistor is virtually an open circuit between collector and emitter.

The central region where the curves are uniform in spacing and slope is called the *active region* (unhatched). In this region, emitter-base junction is forward biased and the collector-base junction is reverse biased. If the transistor is to be used as a linear amplifier, it should be operated in the active region.

If the base current is subsequently driven large and positive, the transistor switches into the saturation region via the active region, which is traversed at a rate that is dependent on factors such as gain and frequency response. In this ON condition, large collector current flows and collector voltage falls to a very low value, called $V_{CEsat}$, typically around 0.2 V for a silicon transistor. The transistor is virtually a short circuit in this state.

High speed switching circuits are designed in such a way that transistors are not allowed to saturate, thus reducing switching times between ON and OFF times.

*Transistor parameters* The slope of the CE characteristics will give the following four transistor parameters. Since these parameters have different dimensions, they are commonly known as common emitter *hybrid parameters* or *h-parameters.*

*(i) Input impedance ($h_{ie}$)*: It is defined as the ratio of the change in (input) base voltage to the change in (input) base current with the (output) collector voltage $V_{CE}$ kept constant. Therefore,

$$h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B}, \quad V_{CE} \text{ constant} \tag{6.18}$$

It is the slope of CE input characteristics $I_B$ versus $V_{BE}$ as shown in Fig. 6.11. The typical value of $h_{ie}$ ranges from 500 to 2000 Ω.

*(ii) Output admittance ($h_{oe}$)*: It is defined as the ratio of change in the (output) collector current to the corresponding change in the (output) collector voltage with the (input) base current $I_B$ kept constant. Therefore,

$$h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}}, \quad I_B \text{ constant} \tag{6.19}$$

It is the slope of CE output characteristic $I_C$ versus $V_{CE}$ as shown in Fig. 6.12. The typical value of this parameter is of the order of 0.1 to 10 μ mhos.

*(iii) Forward current gain ($h_{fe}$)*: It is defined as a ratio of the change in the (output) collector current to the corresponding change in the (input) base current keeping the (output) collector voltage $V_{CE}$ constant. Hence,

$$h_{fe} = \frac{\Delta I_C}{\Delta I_B}, \quad V_{CE} \text{ constant} \tag{6.20}$$

It is the slope of $I_C$ versus $I_B$ curve. Its typical value varies from 20 to 200.

*(iv) Reverse voltage gain ($h_{re}$)*: It is defined as the ratio of the change in the (input) base voltage and the corresponding change in (output) collector voltage with constant (input) base current, $I_B$. Hence,

$$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}}, \; I_B \text{ constant} \tag{6.21}$$

It is the slope of $V_{BE}$ versus $V_{CE}$ curve. Its typical value is of the order of $10^{-5}$ to $10^{-4}$.

### 6.6.3 CC Configuration

The circuit diagram for determining the static characteristics of an NPN transistor in the common collector configuration is shown in Fig. 6.13.

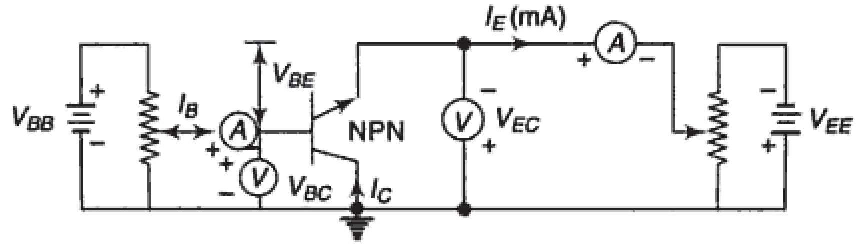


**Fig. 6.13** Circuit to determine CC static characteristics

*Input characteristics* To determine the input characteristics, $V_{EC}$ is kept at a suitable fixed value. The base-collector voltage $V_{BC}$ is increased in equal steps and the corresponding increase in $I_B$ is noted. This is repeated for different fixed values of $V_{EC}$. Plots of $V_{BC}$ versus $I_B$ for different values of $V_{EC}$ shown in Fig. 6.14 are the input characteristics.

*Output characteristics* The output characteristics shown in Fig. 6.15 are the same as those of the common emitter configuration.

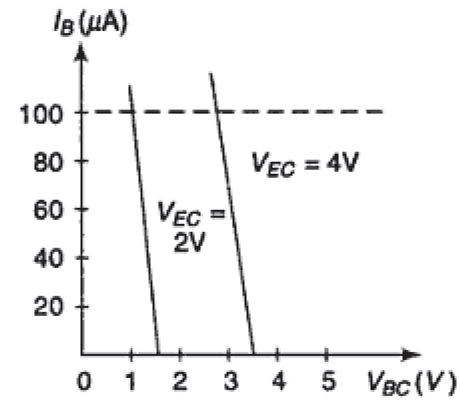


**Fig. 6.14** CC input characteristics

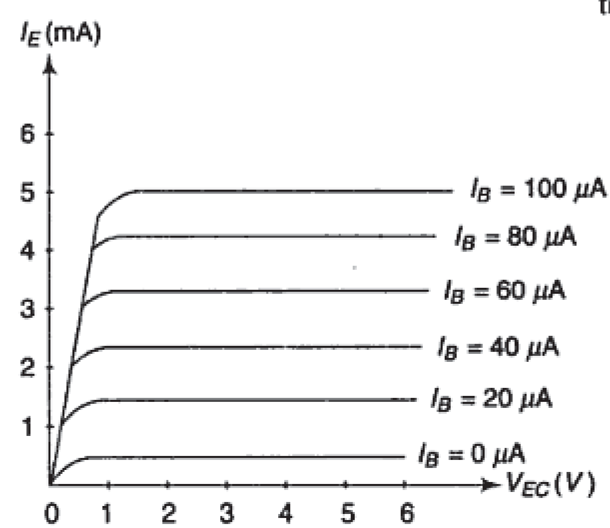


**Fig. 6.15** CC output characteristics

### 6.6.4 Comparison

**Table 6.1** A comparison of CB, CE and CC configurations

| *Property* | *CB* | *CE* | *CC* |
|---|---|---|---|
| Input resistance | Low (about 100 Ω) | Moderate (about 750 Ω) | High (about 750 kΩ) |
| Output resistance | High (about 450 kΩ) | Moderate (about 45 kΩ) | Low (about 25 Ω) |
| Current gain | 1 | High | High |
| Voltage gain | About 150 | About 500 | Less than 1 |
| Phase shift between input & output voltages | 0 or 360° | 180° | 0 or 360° |
| Applications | for high frequency circuits | for audio frequency circuits | for impedance matching |

### 6.6.5 Current Amplification Factor

In a transistor amplifier with a.c. input signal, the ratio of change in output current to the change in input current is known as the current amplification factor.

In the CB configuration the current amplification factor, $\alpha = \dfrac{\Delta I_C}{\Delta I_E}$ (6.22)

In the CE configuration the current amplification factor, $\beta = \dfrac{\Delta I_C}{\Delta I_B}$ (6.23)

In the CC configuration the current amplification factor, $\gamma = \dfrac{\Delta I_E}{\Delta I_B}$ (6.24)